AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 32 with the following amended paragraph:

To fanout, or distribute the bias current to the various delay elements, a current mirror circuit scheme is typically employed. As shown in Figure 2, a conventional current mirror includes a reference current source 19 coupled to a current source transistor QS to generate the same current through a first mirror transistor QFM1 ~~QFM~~. The mirror transistor's gate is tied to its drain, with its source terminal coupled to the supply voltage VDD. A plurality of mirroring transistors QFM2 - QFMN are disposed in parallel, each with its gate tied to the first mirror transistor gate, and source terminals tied to VDD.

Please replace the paragraph beginning on page 5, line 27 with the following amended paragraph:

Referring now to Figure 4, the fanout circuitry 30 ~~generally~~ includes a current mirror CM1. CM1 includes a reference current source input transistor QIN1 that receives an off-chip current IOC to generate a bias voltage ~~for a first current mirror CM1. The first current mirror is~~ CM1 also includes, in the form of a current DAC, ~~having~~ transistors QM1A - QM1N. As is well understood in the art, the current DAC comprises a bank of transistors that are selectively activated to achieve desired characteristics.

Please replace the paragraph beginning on page 5, line 33 with the following amended paragraph:

With continued reference to Figure 4, ~~the first current mirror CM1 (transistor DAC QM1A – QM1N) is~~ Transistors QM1A – QM1N are disposed in series with a second current mirror CM2 comprising transistor QM2, forming a node with QM2 at 40. While not explicitly shown in Figure 4, the voltage-to-current converter output (Figure 3) is connected to node 40. The second current mirror transistor QM2, in turn, has its gate tied to the gates of an array of mirror transistors QM3 - QMN. Because of the respective gate-to-source connections for each transistor, the current through QM2 is duplicated en masse through transistors QM3 - QMN. The duplicated currents are then fed as bias currents to the delay cells, or groups of delay cells.